High-Frequency Equivalent Circuit of GaAs FET's for Large-Signal Applications

Manfred Berroth and Roland Bosch

Abstract—**The application of GaAs field effect transistors in digital circuits requires a valid description by an equivalent circuit at all possible gate and drain bias voltages for all frequencies from dc up to the GHz range. This paper describes an equivalent circuit which takes into account the gate current of positively biased transistors as well as the symmetrical nature of the devices at low drain voltages. A fast method to determine the elements of the equivalent circuit from measured S parameters is presented which delivers for the first time very good agreement for all operating points.**

I. Introduction

THE growing field of GaAs MESFET and MODFET applications requires the development of circuit simulation models. For MMIC designs, small-signal equivalent circuits of the type shown in Fig. 1 have been used up to 60 GHz [1], [2]. Recently developed MODFET's with very high transit frequencies have threshold voltages of about 0 V [3]. The operating point for maximum transconductance and highest transit frequency is at a positively biased gate. However, at these bias points the gate current cannot further be neglected. Another problem occurs in switching applications, when the drain-to-source voltage of the field effect transistor (FET) comes close to 0 V. In this case the symmetrical nature of the physical device has to be reflected in the equivalent circuit. A physically meaningful small-signal equivalent circuit including these features is not only an important tool for circuit design; it will also give important hints for device fabrication and improvement. We propose an extended equivalent circuit together with a fast method to determine its elements from S-parameter measurements for all operating points and without frequency limitations. Only an equivalent circuit which describes the transistor at all bias points precisely can be used to evaluate the bias dependences of the intrinsic circuit elements. This is essential for large-signal applications.

II. The Small-Signal Equivalent Circuit

A complete small-signal equivalent circuit is shown in Fig. 2. The circuit is divided into the external part, with eight parasitic elements, and the intrinsic device, containing nine elements defined by ten variables ($g_m = |g_m| e^{-j\omega\tau}$). All external elements are considered to be constant for all operating points. All intrinsic elements depend on the applied gate and drain voltages. For operating points with positive gate bias, the differential resistances of the gate-to-source and gate-to-drain diodes are modeled by the resistances R_{fs} and R_{fd}. To ensure a smooth transition from the symmetric "cold model" [1], [2], [4] to operating points in the saturation region, the resistor R_{dg} is included. At low drain voltages, the gate-to-drain capacitance is about the same as the gate-to-source capacitance, and the series resistances R_i and R_{gd} determine the real parts of Y_{11i} and Y_{12i} respectively.

Our method to extract the element values from S-parameter measurements is similar to [1] and [5] but is applied to the extended circuit. Furthermore the frequency limitations of [1] and [5] have been overcome by a fully analytic solution of the intrinsic Y-parameter equations as in [7] for the circuit of Fig. 1. First, the external parasitic elements have to be determined by so-called cold modeling at a drain-to-source voltage of 0 V, as described in [1], [2], and [4]. Then "hot" measured S parameters ($V_{ds} > 0$ V) are de-embedded from the external parasitic elements to obtain the equivalent Y parameters of the intrinsic device. The measured S parameters are converted to the corresponding Y and Z parameters by well-known transformations.

Thereafter a fast procedure is applied to determine all voltage-dependent elements of the equivalent circuit at each operating point using an analytic solution of the Y-parameter equations of the intrinsic device. This parameter extraction is referred to as hot modeling. Detailed descriptions of the methods used in the cold and hot modeling processes are given in the following sections.

III. Cold Modeling

For cold modeling, all S-parameter measurements are carried out at 0 V drain-to-source voltage. In this case the transistor is a nonlinear symmetric device. The parasitic gate, source, and drain resistances and inductances are determined first at a far positively biased gate. At these bias points, the following simplified equations, given in [1], are valid:

$$Z_{11} = R_s + R_g + \frac{R_c}{3} + \frac{nkT}{qI_g} + j\omega(L_s + L_g) \tag{1}$$

$$Z_{12} = Z_{21} = R_s + \frac{R_c}{2} + j\omega L_s \tag{2}$$

$$Z_{22} = R_s + R_d + R_c + j\omega(L_s + L_d). \tag{3}$$

R_c is the channel resistance at the applied gate voltage and nkT/qI_g is the differential resistance of the Schottky diode. As there are four unknown resistors and only three equa-

Manuscript received January 16, 1990; revised August 14, 1990.

The authors are with the Fraunhofer Institute for Applied Solid State Physics, D-7800 Freiburg, Germany.

IEEE Log Number 9041079.

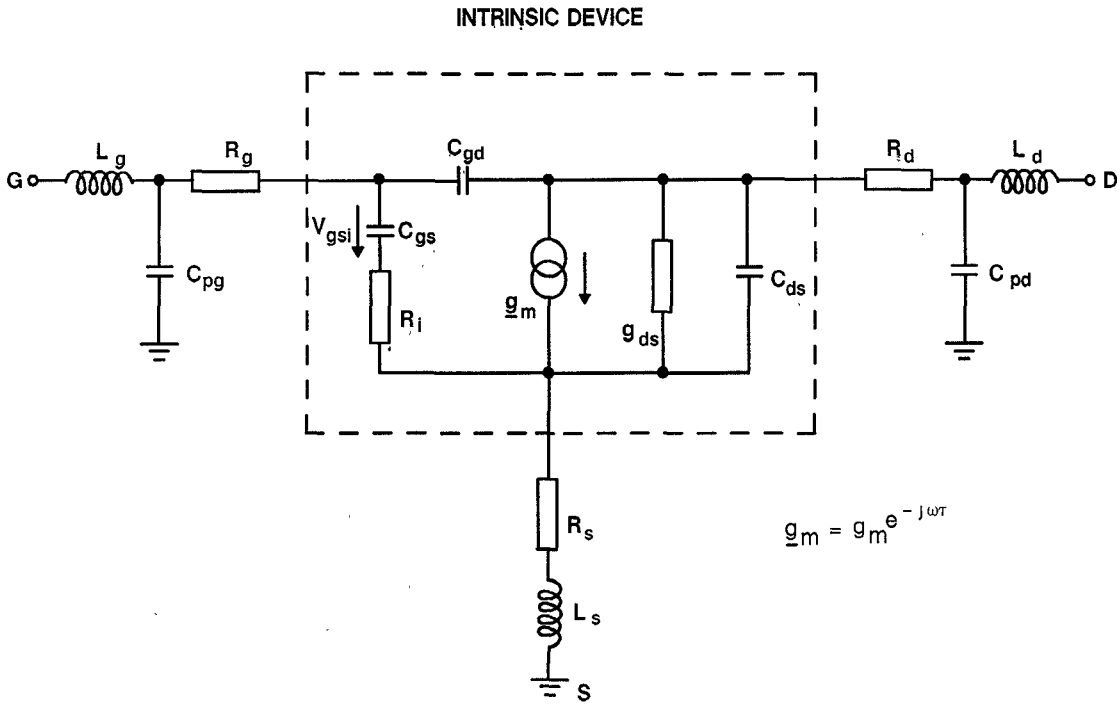


Fig. 1. Small-signal equivalent circuit of a field effect transistor [1].

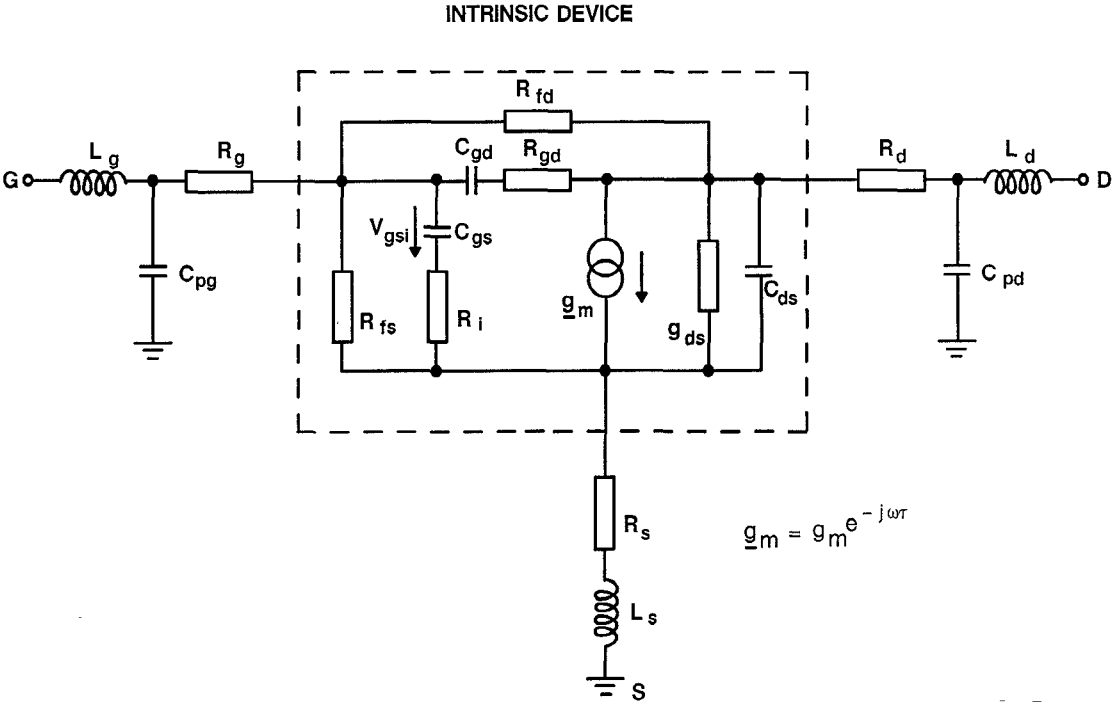


Fig. 2. Extended small-signal equivalent circuit of a field effect transistor including gate current and resistive feedback.

tions with corresponding real parts, one additional relation is required. We use a method similar to that in [6] to determine the sum of R_s and R_d from S-parameter measurements. The three inductances are calculated from the imaginary parts of these equations without making additional assumptions.

The gate and drain pad capacitances C_{pg} and C_{pd} can be extracted from S-parameter measurements at gate voltages below pinch-off using the following simplified equations [1]:

$$\mathrm{Im}(Y_{11}) = j\omega(C_{pg} + 2C_b) \tag{4}$$

$$\mathrm{Im}(Y_{12}) = \mathrm{Im}(Y_{21}) = -j\omega C_b \tag{5}$$

$$\mathrm{Im}(Y_{22}) = j\omega(C_b + C_{pd}). \tag{6}$$

C_b is the residual coupling capacitance from the gate to the source and drain region.

An alternative method is to use transistor designs on the same wafer without active area. From this passive structure, the gate and drain pad capacitances, C_{pg} and C_{pd}, are derived from measured S-parameter data of those metal structures by means of (4) to (6).

IV. Hot Modeling

The measured S-parameter data can be transferred to the corresponding Z and Y parameters for any bias and frequency. By means of these transformations, the S-parameter data can be de-embedded from the parasitic external elements, as shown in [1]. The intrinsic device (Fig. 2) can be described by the following four complex Y-parameter equations:

$$Y_{11i} = g_{fs} + g_{fd} + \frac{\omega^2 R_i C_{gs}^2}{D1} + \frac{\omega^2 R_{gd} C_{gd}^2}{D2} + j\omega\left(\frac{C_{gs}}{D1} + \frac{C_{gd}}{D2}\right) \tag{7}$$

$$Y_{12i} = -g_{fd} - \frac{\omega^2 R_{gd} C_{gd}^2}{D2} - j\omega\frac{C_{gd}}{D2} \tag{8}$$

$$Y_{21i} = -g_{fd} + \frac{g_m e^{-j\omega\tau}}{1 + j\omega R_i C_{gs}} - j\frac{\omega C_{gd}}{1 + j\omega R_{gd} C_{gd}} \tag{9}$$

$$Y_{22i} = g_{fd} + g_{ds} + \frac{\omega^2 R_{gd} C_{gd}^2}{D2} + j\omega\left(C_{ds} + \frac{C_{gd}}{D2}\right) \tag{10}$$

where

$$D1 = 1 + \omega^2 C_{gs}^2 R_i^2 \tag{11}$$

$$D2 = 1 + \omega^2 C_{gd}^2 R_{gd}^2 \tag{12}$$

$$g_{fs} = \frac{1}{R_{fs}} \tag{13}$$

$$g_{fd} = \frac{1}{R_{fd}}. \tag{14}$$

By separating these equations into their real and imaginary parts, eight circuit elements can be determined. However, in our equivalent circuit (Fig. 2) the intrinsic transistor is modeled by ten intrinsic variables. As additional relations for the differential resistances R_{fs} and R_{fd}, either dc measurements or S-parameter measurements at very low frequencies can be used. As can be seen from (7) and (8), the real parts of the intrinsic Y parameters Y_{11i} and Y_{12i} diminish at low frequencies, with the exception of g_{fs} and g_{fd}. The differential conductances of the gate diodes, g_{fs} and g_{fd}, can therefore be determined at each operating point at low frequencies, e.g. 50 MHz, by the following equations:

$$g_{fd} = -\mathrm{Re}(Y_{12i}) \tag{15}$$

$$g_{fs} = \mathrm{Re}(Y_{11i}) - g_{fd}. \tag{16}$$

At the same bias point the remaining eight parameters can be calculated for each measured frequency independently. After separating (7) through (10) into their real and imaginary parts, the expressions for the elements of the small-signal equivalent circuit turn out to be (see the Appendix)

$$C_{gd} = -\frac{\mathrm{Im}(Y_{12i})}{\omega}\left(1 + \left(\frac{\mathrm{Re}(Y_{12i}) + g_{fd}}{\mathrm{Im}(Y_{12i})}\right)^2\right) \tag{17}$$

$$R_{gd} = \frac{\mathrm{Re}(Y_{12i}) + g_{fd}}{\omega C_{gd}\,\mathrm{Im}(Y_{12i})} \tag{18}$$

$$C_{gs} = \frac{\mathrm{Im}(Y_{11i}) + \mathrm{Im}(Y_{12i})}{\omega}\left(1 + \frac{\left(\mathrm{Re}(Y_{11i}) + \mathrm{Re}(Y_{12i}) - g_{fs}\right)^2}{\left(\mathrm{Im}(Y_{11i}) + \mathrm{Im}(Y_{12i})\right)^2}\right) \tag{19}$$

$$R_i = \frac{\mathrm{Re}(Y_{11i}) + \mathrm{Re}(Y_{12i}) - g_{fs}}{\omega C_{gs}(\mathrm{Im}(Y_{11i}) + \mathrm{Im}(Y_{12i}))} \tag{20}$$

$$g_m = \sqrt{\left((\mathrm{Re}(Y_{21i}) - \mathrm{Re}(Y_{12i}))^2 + (\mathrm{Im}(Y_{21i}) - \mathrm{Im}(Y_{12i}))^2\right)D1} \tag{21}$$

$$\tau = \frac{1}{\omega}\arcsin\left(\frac{\mathrm{Im}(Y_{12i}) - \mathrm{Im}(Y_{21i}) - \omega C_{gs} R_i(\mathrm{Re}(Y_{21i}) - \mathrm{Re}(Y_{12i}))}{g_m}\right) \tag{22}$$

$$C_{ds} = \frac{\mathrm{Im}(Y_{22i}) + \mathrm{Im}(Y_{12i})}{\omega} \tag{23}$$

$$g_{ds} = \mathrm{Re}(Y_{22i}) + \mathrm{Re}(Y_{12i}). \tag{24}$$

Equations (17) through (24) are valid

i) for drain voltages greater than 0 V,
ii) for positive and negative gate voltages,
iii) for all frequencies for which the equivalent circuit is valid.

As there are no time-consuming iteration loops in the hot modeling procedure, this method can effectively be used for on-wafer S-parameter measurements with real-time parameter extraction.

V. Measurements and Results

Several different types of FET's have been investigated to verify our method and to compare it with the results of other procedures. We examined heterostructure FET's as well as MESFET's fabricated at our institute. The hot modeling

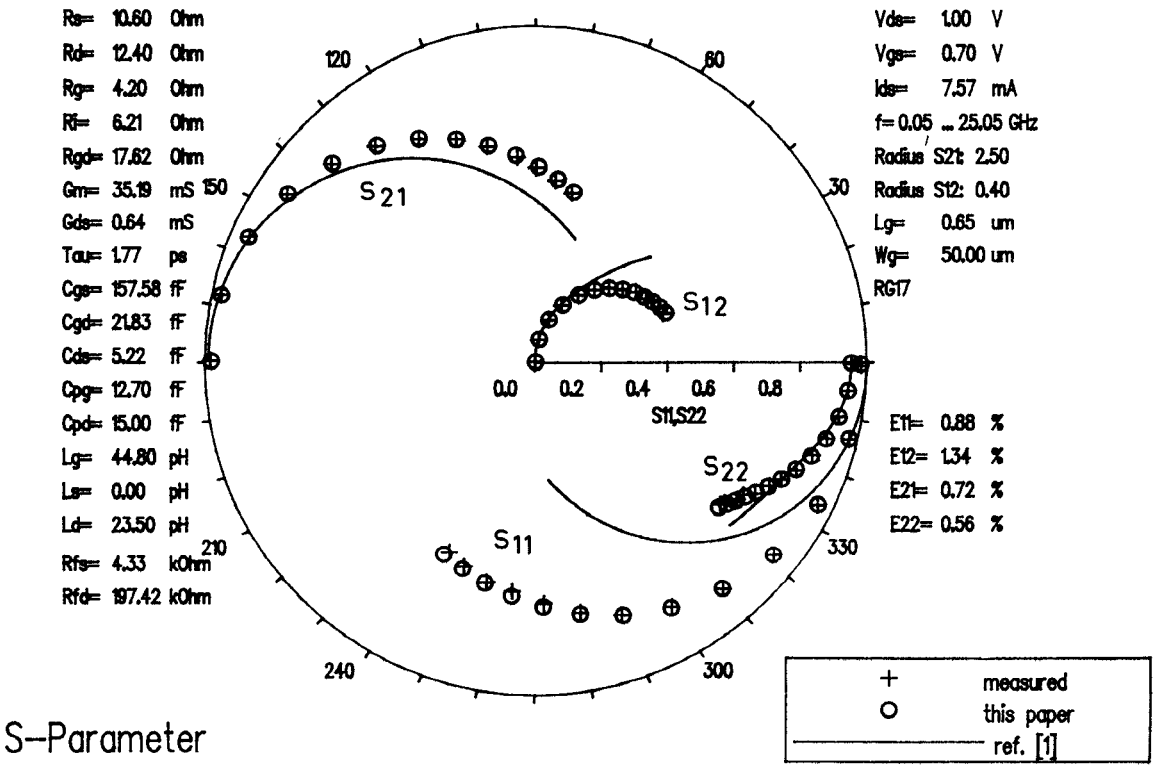


Fig. 3. Comparison of measured data of a 0.6 μm enhancement heterostructure field effect transistor (crosses) with simulation results of our procedure (circles) and the method proposed in [1] (solid lines) at positive gate bias.

method, described in [1], is limited to frequencies below 5 GHz, which is a severe limitation for present and future applications of GaAs FET devices. We compared the method described in [1] with our fully analytical approach up to our measurement limit, and the results shown in Fig. 3. The crosses indicate the measured S parameters of a heterostructure FET with pulse doped layers on both sides of the undoped channel with a gate length of 0.6 μm. The gate and drain voltages were +0.7 V and 1.0 V, respectively. The solid line represents the results of the method described in [1], and the circles show the results of our method. Obviously, our model yields better agreement with the measured data at high frequencies, showing that extrapolations of our model to higher frequencies are more reliable. The low error averages, E_{ij}, of our improved model should be noted.

Fig. 4 presents the intrinsic capacitances as calculated for the operating point given in Fig. 3. We can use this plot to verify the validity of the equivalent circuit at high frequencies. The equivalent circuit remains valid as long as its elements turn out to be independent of frequency, with the deviation from the mean value being an indication of the error of this element value.

As a further example, Fig. 5 shows a depletion-type heterostructure FET with a gate voltage of 0.6 V and a drain voltage of 0.05 V. These low drain voltages occur in switching applications of FET's. Again, our proposed method (circles) neatly approximates the measured data, while the solid line according to [1] cannot fit in particular the S_{11} and S_{12} data points. As the influence of the differential resistances is not considered in [1], the method cannot be used for operating points with a significant gate current.

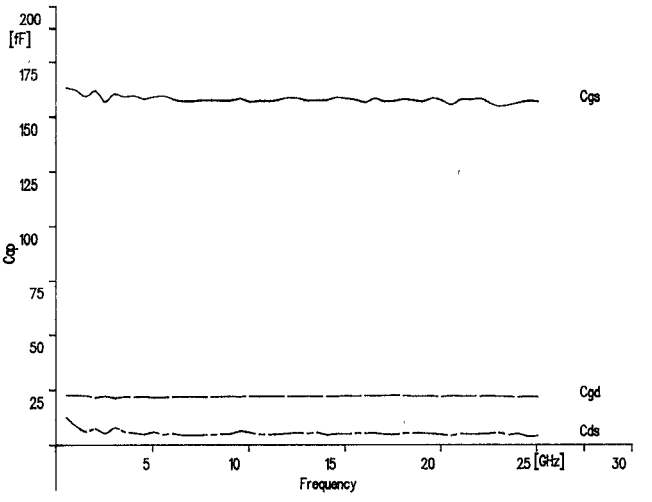


Fig. 4. The intrinsic capacitances C_{gs}, C_{gd}, and C_{ds} versus frequency calculated at the same bias conditions as in Fig. 3.

As the accuracy of our parameter extraction is high and the computation time is well under a second on a μVAX II, we can calculate the small-signal equivalent circuit elements at many operating points. Thus the bias dependences of all internal elements are quickly established. Owing to the validity of the equivalent circuit for all operating points, these voltage dependences of the equivalent circuit elements can be utilized for large-signal model development. The implementation of this model into SPICE will be reported elsewhere.

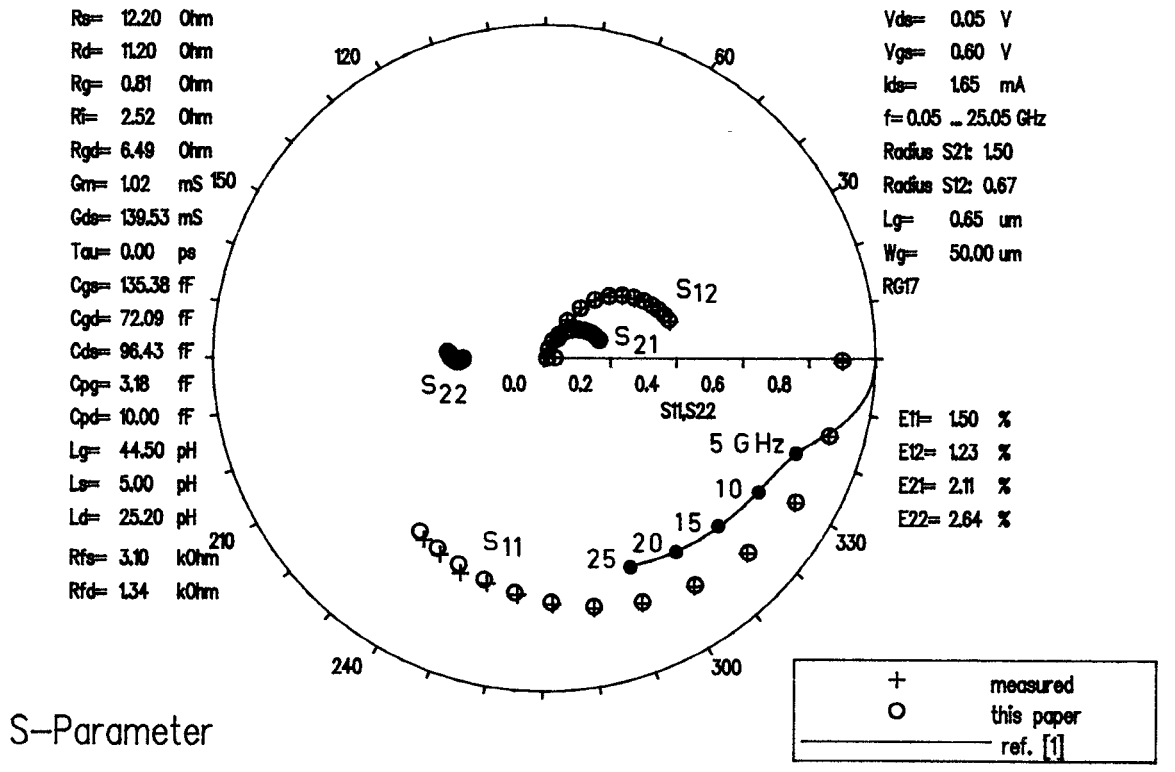


Fig. 5. Comparison of measured data of a 0.6 μm depletion heterostructure field effect transistor (crosses) with simulation results of our procedure (circles) and the method proposed in [1] (solid lines) at low drain voltages.

VI. Conclusion

An extended small-signal equivalent circuit for GaAs field effect transistors is proposed. It includes the effects of the differential resistances of the gate-to-source and gate-to-drain diodes as well as the serial resistance of the feedback capacitance. A fast and accurate method to determine all elements of this equivalent circuit at all bias points without frequency limitations is presented. Direct computation from analytical expressions, without iteration, allows this parameter extraction procedure to be used for real-time on-wafer parameter extraction. Large-signal calculations are possible by inserting the voltage dependences evaluated for the elements into suitable simulation programs such as SPICE.

Appendix

With the exception of g_m and τ, all circuit variables can be determined by simple algebraic operations. To solve for g_m and τ we have to use (9):

$$Y_{21i} = -g_{fd} + \frac{g_m e^{-j\omega\tau}}{1+j\omega R_i C_{gs}} - j\frac{\omega C_{gd}}{1+j\omega R_{gd} C_{gd}} \tag{A1}$$

which can be rewritten as

$$Y_{21i} = \frac{g_m(1-j\omega R_i C_{gs})(\cos(\omega\tau) - j\sin(\omega\tau))}{1+(\omega R_i C_{gs})^2} + Y_{12i}. \tag{A2}$$

We can separate the real and imaginary parts:

$$\mathrm{Re}(Y_{21i}) = \frac{g_m(\cos(\omega\tau) - \omega R_i C_{gs}\sin(\omega\tau))}{1+(\omega R_i C_{gs})^2} + \mathrm{Re}(Y_{12i}) \tag{A3}$$

$$\mathrm{Im}(Y_{21i}) = -\frac{g_m(\omega R_i C_{gs}(\cos(\omega\tau) + \sin(\omega\tau))}{1+(\omega R_i C_{gs})^2} + \mathrm{Im}(Y_{12i}). \tag{A4}$$

For simplification of the notation, we use

$$\mathrm{R} = \mathrm{Re}(Y_{21i}) - \mathrm{Re}(Y_{12i}) \tag{A5}$$

$$\mathrm{I} = \mathrm{Im}(Y_{21i}) - \mathrm{Im}(Y_{12i}) \tag{A6}$$

$$\phi = \omega\tau \tag{A7}$$

$$b = \omega C_{gs} R_i \tag{A8}$$

$$a = \frac{g_m}{1+b^2}. \tag{A9}$$

Then we get

$$\mathrm{R} = a(\cos\phi - b\sin\phi) \tag{A10}$$

$$\mathrm{I} = -a(b\cos\phi + \sin\phi) \tag{A11}$$

This can be written as

$$\cos\phi = \frac{\mathrm{R}}{a} + b\sin\phi. \tag{A12}$$

Now we can solve for ϕ:

$$\sin\phi = \frac{-\mathrm{I} - b\mathrm{R}}{a(1+b^2)}. \tag{A13}$$

Inserting (A13) into (A10) and using $\cos\phi = \sqrt{1-\sin^2\phi}$ yields

$$a = \sqrt{\frac{I^2+R^2}{1+b^2}}. \tag{A14}$$

By resubstitution, we get g_m and τ:

$$g_m = \sqrt{\left(\left(\mathrm{Re}(Y_{21i}) - \mathrm{Re}(Y_{12i})\right)^2 + \left(\mathrm{Im}(Y_{21i}) - \mathrm{Im}(Y_{12i})\right)^2\right) D1} \tag{A15}$$

$$\tau = \frac{1}{\omega}\arcsin\left(\frac{\mathrm{Im}(Y_{12i}) - \mathrm{Im}(Y_{21i}) - \omega C_{gs} R_i\left(\mathrm{Re}(Y_{21i}) - \mathrm{Re}(Y_{12i})\right)}{g_m}\right). \tag{A16}$$

Acknowledgment

The authors would like to thank Dr. W. H. Haydl and Dr. V. Hurm for stimulating discussions of this work as well as Mr. W. Benz for assistance in dc measurements. Thanks are also due to our colleagues who prepared and fabricated the samples.

References

[1] G. Dambrine, A. Cappy, F. Heliodore, and E. Playez, "A new method for determining the FET small-signal equivalent circuit," *IEEE Trans. Microwave Theory Tech.*, vol. 36, pp. 1151–1159, July 1988.

[2] W. R. Curtice and R. L. Camisa, "Self-consistent GaAs FET models for amplifier design and device diagnostics," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-32, pp. 1573–1578, Dec. 1984.

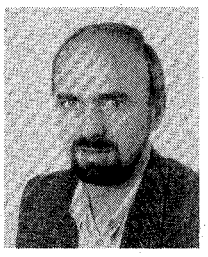
[3] Loi D. Nguyen *et al.*, "Influence of quantum-well width on device performance of $Al_{0.30}Ga_{0.70}As/In_{0.25}Ga_{0.75}As$ (on GaAs) MODFET's," *IEEE Trans. Electron Devices*, vol. 36, pp. 833–838, May 1989.

[4] T.-H. Chen and M. Kumar, "Novel GaAs FET modelling technique for MMICs," in *1988 GaAs IC Symp. Tech. Dig.* (Nashville), Nov. 1988, pp. 49–52.

[5] R. A. Minasian, "Simplified GaAs MESFET model to 10 GHz," *Electron. Lett.*, vol. 13, no. 8, pp. 549–551, 1977.

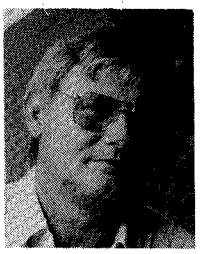
[6] P. L. Hower and N. G. Bechtel, "Current saturation and small-signal characteristics of GaAs field effect transistors," *IEEE Trans. Electron Devices*, vol. ED-20, pp. 213–220, Mar. 1973.

[7] M. Berroth and R. Bosch, "Broad-band determination of the FET small-signal equivalent circuit," *IEEE Trans. Microwave Theory Tech.*, vol. 38, pp. 891–895, July 1990.



Manfred Berroth was born at Obersontheim, West Germany, in 1956. He received the Dipl.-Ing. degree from the University of the Federal Armed Forces, Munich, in 1979.

He then developed microprocessor systems and dedicated image processing software as a consultant. In 1987, he joined the Institute for Applied Solid State Physics, in Freiburg, Germany, where he is currently engaged in the development of circuit simulation models for GaAs field effect transistors as well as integrated circuit design.



Roland Bosch was born in Stuttgart, Germany, on April 7, 1937. He studied at the Technical University of Stuttgart and the Albert Ludwig University of Freiburg, Germany, and received the Diplom-Physiker degree in 1964.

Since then he has been employed at the Fraunhofer-Institute for Applied Solid-State Physics, Freiburg, Germany. He carried out theoretical and experimental work on the Gunn effect in GaAs and subsequently was engaged in making InP Gunn diodes for millimeter-wave applications. Currently he is involved in GaAs microwave FET and MMIC research and development projects. His work focuses mainly on microwave measurements of active and passive components and on the evaluation of equivalent circuits.